

8 with the voltage ramp, said operational amplifier operating in a linear  
9 mode, whereby said output voltage approximates a multiple of the  
10 voltage ramp;  
11 d. transistor means electronically connected to said operational amplifier  
12 circuit, said transistor means operating in linear mode during capacitor  
13 charging, and subsequently reaching a full-ON state; and  
14 e. energy storage load means connected to said transistor means for  
15 receiving a full power supply after said transistor means reaches its  
16 said full-ON state.

☒ Please cancel claims 5 and 9 – 16, and add the following new claims:

1 ~~17.~~<sup>8.</sup> The inrush circuit of claim 1, further comprising time delay means connected to  
2 said means for providing a voltage ramp.

1 ~~18.~~<sup>9.</sup> The inrush circuit of claim ~~17~~<sup>8</sup>, wherein said time delay means reaches threshold in  
2 about 50 ms.

1 ~~19.~~<sup>10.</sup> The inrush circuit of claim 1, wherein said energy storage load means is a bulk  
2 capacitor.